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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,253	09/01/2000	Cynthia L. Recker	SC11244ZC	5727

23330 7590 02/26/2004

MOTOROLA, INC.
CORPORATE LAW DEPARTMENT - #56-238
3102 NORTH 56TH STREET
PHOENIX, AZ 85018

EXAMINER	
ROSALES HANNER, MORELLA I	
ART UNIT	**PAPER NUMBER**
2128	3

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/654,253	RECKER ET AL.	
	Examiner	Art Unit	
	Morella I Rosales-Hanner	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *01 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☑ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Claims 1 – 20 have been examined.

Drawings

2. The drawings submitted on 09/01/2000 are acceptable.

Specification

3. The attempt to incorporate the following subject matter into this application by reference:

- a paper by P. Drennan and C. McAndrew, titled 'A comprehensive MOSFET Mismatch Model', IEEE ICMTS, 2000 [**Pg 3, line 21**] and
- a Ph.D. dissertation by P. Drennan, titled 'Integrated Circuit Device Mismatch Modeling and Characterization for Analog Circuit Design', Arizona State University, May 1999 [**Pg 4, line 3**]

Is improper because it attempts to incorporate essential material by referring to non-U.S patent material [see MPEP 6.19.01].

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 1 – 20** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claims recite, "Mismatch model" namely the formula which is disclosed on line 19, page 3 of the specification. However, the specification fails to disclose or define all of the symbols listed in the formula, specifically P_j.

Claim Rejections – 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.1. Claims 1 – 6 and 8 - 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **[(***Drennan* "Integrated Circuit Device Mismatch Modeling and Characterization for Analog Circuit Design" PhD dissertation**)** or **(***McAndrew* "Practical Modeling for Circuit Simulation**"** article**)** or **(**Drennan et al. "A Comprehensive MOSFET Mismatch Model"**)]** in view of Rostoker et al. (U.S. Patent No. 5,867,399) hereafter referred to as *Rostoker*.

Drennan teaches:

- general mismatch principles [**Chapter 3, Pg 31**],
- a method for resistor mismatch [**Chapter 4, Pg 4**],
- a method for MOSFET mismatch [**Chapter 5, Pg 105**]
- and a method for BJT mismatch [**Chapter 6, Pg 196**].

McAndrew teaches that mismatch is one of the major causes of yield loss for analog circuits [**Pg 439, Col 2, part II**] and there has been an intense effort to increase the accuracy of MOSFET models.

McAndrew also teaches the importance of being able to quickly retarget a design library when a process change occurs [**Pg 440, part IV, paragraph 2**] and that for one **Motorola** process, models extrapolated from a previous generation process, based on changes on process parameters that control electrical behavior and geometric design parameters, were more accurate than predictions from process and device simulations. The design library disclosed by *McAndrew* is equivalent to the to the editable mismatch model data library claimed by the applicant, for example, in claims 1 [**line 3**] and 10 [**line 3**].

McAndrew further teaches [**Pg 447, part X, line 6**] that the considerable effort and expense required to develop a compact model, that is characterized and implemented in a circuit simulator, can be wasted if the practical aspects of getting complete models working in a CAD system on a computer on the designer's desk are ignored.

Drennan et al. teaches a comprehensive mismatch model based on physical process parameters and characterization. *Drennan et al.* further teaches [**Conclusion,**

sentence 4] that a unique and powerful advantage of the disclosed mismatch model is the analysis of the contributions of the process parameters to the overall mismatch allows identification of the important physical root causes of mismatch, which can be used to guide process diagnosis and improvement.

The base references do not expressly teach implementation of the mismatch model in a GUI.

Rostoker discloses a [Col 6, line 28] an ECAD system whereby the characteristics of schematic editor, schematic compiler, and simulator are all presented to the user in a fashion such that they appear as a single, integrated function in a GUI.

Rostoker teaches **[col 4, line 16]** that simulation is often provided by utilizing simulation models at one or more of several different levels. *Rostoker* also teaches **[col 4, line 46]** that the simulation model used by the simulator is usually derived from the output of the schematic editor by a schematic compiler, also making use of information about performance characteristics of the circuits, often stored in simulation libraries. These simulation libraries are equivalent to the circuit simulation library claimed by the applicant, for example, in claim 1 **[lines 6 - 7]** and claim 10 **[lines 6 - 7]**.

Rostoker further teaches [Col 9, line 4] a graphical user interface that allows a user to interacts with the ECAD system, whereby the user may create, select, move, modify and delete objects on the display screen, where objects may represent circuit components, wires, commands, text values, or any other visual representation of data. Refer to FIGS. 13 through 15 for representative screen displays of the methodology of the system disclosed by *Rostoker*, as they would be presented to the user. This

graphical user interface is equivalent to the graphical interface claimed by the applicant in independent claim 1 [**lines 9 –20**], dependent claim 11.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to implement the transistor mismatch model disclosed by the base references in a CAD system on a computer utilizing a design library and a simulation library and graphical user interface as disclosed by *Rostoker* in order to develop more complete, accurate, numerically robust models that work properly with the numerical algorithms in simulators and with other CAD tools in an IC design system and improve the quality of modeling in the semiconductor industry. Furthermore, McAndrew states that the considerable effort and expense required to develop a compact model, that is characterized and implemented in a circuit simulator, can be wasted if the practical aspects of getting complete models working in a CAD system on a computer on the designer's desk are ignored. Finally, most computers, at the time of this invention, have a GUI interface thus it would be reasonable to expect a GUI interface.

6. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over (*Drennan* or *McAndrew* or *Drennan et al) in* view of *Rostoker,* as applied in section 5, further in view of U.S Patent No. U.S. 5,826,269 to Peter Hussey, hereafter referred to as *Hussey.*

The base references do not expressly disclose an e-mailed ASCII output data file.

Hussey discloses [**Col 3, line 27**] an electronic mail interface that provides an efficient networked system that processes user requests submitted to a network server,

the results of which are typically viewed at a later time in order to facilitate task scheduling by the server of user requests from connected client computers in a network, and thereby reduce the incidence of system bottlenecks that may rise with a server.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to modify the mismatch model disclosed by the base references to email the output data to the user as taught by *Hussey* in order to facilitate task scheduling and thereby reduce the incidence of system bottlenecks. Furthermore, in order to provide complete mismatch models working in a CAD system on a computer on the designer's desk.

Conclusion

7. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- "Transistor matching in analog CMOS applications" by Marcel J.M. Pelgrom, Hans P. Tuinhout and Maarten Vertregt, IEDM 1998 Technical Digest International 6 –9 Dec. 1998 Pg 915-918.
- "Automated Generation of SPICE Characterization Test Masks and Test Databases", by Leo Kasel, Colin C. McAndrew, Patrick Drennan, William F. Davis and Richard Ida, Proc. IEEE Int. Conf. On Microelectronics Test Structures Vol. 12, March 1999, Pgs 74 – 79.
- "Compact Device Modeling for Circuit Simulation", by Colin C. McAndrew, IEEE 1997 Custom Integrated Circuits Conference, Pgs 151 – 158.

- "A New Five-Parameter MOS Transistor Mismatch Model", by Teresa Serrano-Gotarredona and Bernabe Linares-Barranco, IEEE Electron device Letters, Vol 21, No. 1, Jan 2000, Pgs 37 – 39,
- "E-mail at work" Special Report/Electronic Mail, IEEE Spectrum, October 1992, Pgs. 24 – 28.
- Four page printout from Webopedia.com (date unknown): discloses common meaning of "frame".

Response Guidelines

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Morella I Rosales-Hanner whose telephone number is (703) 305-8883. The examiner can normally be reached on Monday – Friday from 7:00 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska, can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MRH
January 29, 2004

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100